RECEIVED
CENTRAL FAX CENTER
MAY 0 2 2007

MCCARTHY & ASSOCIATES
500 WEST MAIN STE. 609
OKLAHOMA CITY, OKLAHOMA 73102
TELEPHONE: (405) 601-2798
FAX: (405) 601-2853

FACSIMILE TRANSMISSION COVER SHEET

DATE: May 2, 2007

NUMBER OF PAGES INCLUDING THIS COVER SHEET: 25

FROM: Mitchell K. McCarthy, Registration No. 38,794

TO: Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ADDRESSEE/ORGANIZATION	FAX NUMBER	TELEPHONE NUMBER
Art Group 2182	(571) 273-8300	(571) 272-4100

RE: **Application No.** **09/494,787**
In re application of: **John A. Mount**
Assignee: **SEAGATE TECHNOLOGY LLC**
Dkt. No.: **STL-09274**

IF YOU DO NOT RECEIVE ALL OF THE PAGES OR IF ANY ARE ILLEGIBLE, PLEASE CONTACT US AT (405) 601-2798 AS SOON AS POSSIBLE.

****

Transmission by Facsimile on May 2, 2007 **PATENT**
Practitioner's Docket No. STL9274

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **John A. Mount**
Application No.: **09/494,787** Group No.: **2182**
Filed: **01/31/2000** Examiner: **Eron Sorrell**
For: **AUTOMATED REGISTER DATA TRANSFER TO REDUCE PROCESSING BURDEN ON A PROCESSING DEVICE**

Mail Stop Appeal Briefs – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

TRANSMITTAL OF APPEAL BRIEF
(PATENT APPLICATION–37 C.F.R. § 41.37)

1. Transmitted herewith, is the APPEAL BRIEF in this application, with respect to the Notice of Appeal filed on February 10, 2007.

2. STATUS OF APPLICANT

This application is on behalf of other than a small entity.

3. FEE FOR FILING APPEAL BRIEF

Pursuant to 37 C.F.R. § 41.20(b)(2), the fee for filing the Appeal Brief is:

other than a small entity	$500.00
Appeal Brief fee due	**$500.00**

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*

I hereby certify that, on the date shown below, this correspondence is being:

MAILING

☐ deposited with the United States Postal Service in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

37 C.F.R. § 1.8(a)
☐ with sufficient postage as first class mail.

37 C.F.R. § 1.10*
☐ as "Express Mail Post Office to Addressee"
Mailing Label No. _____ (mandatory)

TRANSMISSION

☑ facsimile transmitted to the Patent and Trademark Office, (571) 273 - 8300.

Jade Rachelle Caldwell
Signature

Date: May 2, 2007

Jade Rachelle Caldwell
(type or print name of person certifying)

RECEIVED
CENTRAL FAX CENTER
MAY 0 2 2007

4. EXTENSION OF TERM

The proceedings herein are for a patent application and the provisions of 37 C.F.R. § 1.136 apply.

Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

Appeal brief fee	$500.00
Extension fee (if any)	$0.00
TOTAL FEE DUE	**$500.00**

6. FEE PAYMENT

Authorization is hereby made to charge the amount of $500.00 to Credit card as shown on the attached credit card information authorization form PTO-2038

7. FEE DEFICIENCY

If any additional extension and/or fee is required, and if any additional fee for claims is required, charge Deposit Account No. 50-4124.

Date: 5/2/2007

Mitchell K. McCarthy
Registration No. 38,794
McCarthy & Associates
500 West Main Street Ste. 609
Oklahoma City, OK 73102
405-601-2798

Transmission by Facsimile on May 2, 2007

PATENT
Dkt. STL09274

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **John A. Mount**
Assignee: **Seagate Technology LLC**
Filed: **January 31, 2000** Group Art: **2182**
Application No.: **09/494,787** Examiner: **Eron Sorrell**
For: **AUTOMATED REGISTER DATA TRANSFER TO REDUCE PROCESSING BURDEN ON A PROCESSING DEVICE**

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, Virginia 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

Sir:

APPELLANT'S BRIEF

This Brief is in furtherance of the Notice of Appeal filed on February 10, 2007 and following the Pre-Brief Panel's Decision of April 2, 2007. The required fees, any required petition for extension of time for filing this Brief, and the authority and time limits established by the Notice of Appeal are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

CERTIFICATION UNDER 37 C.F.R. §§ 1.8(a) and 1.10*

I hereby certify that, on the date shown below, this correspondence is being:

TRANSMISSION

☐ facsimile transmitted to the Patent and Trademark Office, (571) 273 - 8300.

Jade Rachelle Caldwell
Signature

Date: May 2, 2007

Jade Rachelle Caldwell
(type or print name of person certifying)

05/03/2007 TL0111 00000018 09494787
01 FC:1402 500.00 OP

This brief contains these items under the following headings, and in the order set forth below:

I. REAL PARTY IN INTEREST

The real party in interest in this application is Seagate Technology LLC.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

The status of the claims in this application is:

Claim	Status
1. (Previously presented)	Independent.
2. (Original)	Depends from claim 1.
3. (Original)	Depends from claim 2.
4. (Previously presented)	Depends from claim 1.
5. (Previously presented)	Depends from claim 1.
6. (Original)	Independent.
7. (Original)	Depends from claim 6.
8. (Original)	Depends from claim 6.
9. (Original)	Depends from claim 8.
10. (Original)	Depends from claim 6.
11. (Original)	Depends from claim 6.
12. (Original)	Depends from claim 6.
13. (Original)	Depends from claim 12.
14. (Original)	Depends from claim 6.
15. (Previously presented)	Independent.

16. (Previously presented)	Independent.
17. (Previously presented)	Depends from claim 16.
18. (Previously presented)	Depends from claim 16.
19. (Previously presented)	Depends from claim 16.
20. (Previously presented)	Depends from claim 16.
21. (Previously presented)	Independent.
22. (Previously presented)	Depends from claim 21.
23. (Previously presented)	Depends from claim 21.
24. (Previously presented)	Depends from claim 23.
25. (Previously presented)	Depends from claim 21.

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application: 1-25.

B. STATUS OF ALL THE CLAIMS

1. Claims canceled: none
2. Claims withdrawn from consideration but not canceled: none
3. Claims pending: 1-25
4. Claims allowed: 6-15
5. Claims rejected: 1-5 and 16-25.
6. Claims objected to: none

C. CLAIMS ON APPEAL

Claims now on appeal: 1-5 and 16-25.

IV. STATUS OF AMENDMENTS

Appellant requested a Pre-Brief Panel Review on the basis that this case is not in condition for appeal.[1] The Panel decided to proceed to appeal without comment.[2]

[1] Appellant's Response of 2/10/2007
[2] Decision of 4/2/2007

V. SUMMARY OF CLAIMED SUBJECT MATTER

Embodiments of the present invention as recited by the language of independent claim 1 contemplate an apparatus having a bus (such as 360 in FIG. 3, see pg. 8 lines 10-11) operatively coupled to a first controller chip (such as 200, see pg. 8 line 5) and a first channel chip (such as 300, see pg. 8 line 9-10). The channel chip has several registers (such as 340, see pg. 8 lines 9-10). The apparatus also has a storage medium (such as 500, see pg. 8 lines 20-21) operatively coupled to the bus through a storage medium interface (such as interface 450 of eblock 400, see pg. 8 lines 13-15). A method is provided for retrieving data recorded on the storage medium by retrieving a first portion of the recorded data via the bus (such as block 23 in FIG. 5, see pg. 9 line 14). Some of the registers are then updated via the bus (such as block 24, see pg. 9 line 15). Finally, a second portion of the recorded data is retrieved via the bus (such as blocks 27 and 23, see pg. 9 lines 16-20).

Embodiments of the present invention as recited by the language of dependent claims of independent claim 1 contemplate the interface having a read head (such as 460, 461 of the eblock 400, see pg. 8 lines 11-12). The method further contemplates repositioning the storage medium interface with respect to the storage medium between the retrieving the first portion of data step and the retrieving the second portion of data step (such as block 63 in FIG. 9 which occurs before the head stops radial movement in block 67, see pg. 11 line 21 to pg. 12 line 7).

Furthermore, the interface can have a plurality of operating parameters (such as 440, 441, see pg. 8 lines 11-13) that are modified during the updating the registers step (such as block 26 in FIG. 5, see pg. 9 lines 14-16). The registers can contain at least one read channel parameter value selected from the group consisting of a precompensation value (such as bias 231, 251 or gain 232, 252, see pg. 5 lines 23-30), a filter coefficient value (such as first-order

coefficients 236, 256 or third-order coefficients 237, 257, see pg. 6 lines 2-5), or a phase offset value (such as one of the bits in 238, 258 indicating phase acquisition mode, see pg. 6 line 28), or a mode-indicative value (such as one of the bits in 238, 258 indicating skew compensation mode, see pg. 6 lines 28-29).

Embodiments of the present invention as recited by the language of independent claim 16 contemplate a method for retrieving data recorded on a storage medium by retrieving a first portion of the recorded data via a bus (such as block 23 in FIG. 5, see pg. 9 line 14). Some of the registers are then updated via the bus (such as block 24, see pg. 9 line 15). Finally, a second portion of the recorded data is retrieved via the bus (such as blocks 27 and 23, see pg. 9 lines 16-20).

Embodiments of the present invention as recited by the language of dependent claims of independent claim 16 contemplate the bus being either serial or parallel (see pg. 2 line 25 to pg. 3 line 3). The method steps can be controlled by a processor (such as microcontroller 210 in FIG. 3) and a direct memory access apparatus (such as 220, see pg. 11 line 22 to pg. 12 line 7).

Embodiments of the present invention as recited by the language of independent claim 21 contemplate a method for reducing processing burden on a processing device (such as microcontroller 210 in FIG. 3, see pg. 11 line 29 to pg. 12 line 3). The method provides for transmitting first data via a bus (such as 360 in FIG. 3) coupled to the processing device (such as block 23 in FIG. 5, see pg. 9 line 14). At least one register or parameter is then updated via the bus (such as block 24, see pg. 9 line 15). Finally, second data is transmitted via the bus (such as blocks 27 and 23, see pg. 9 lines 16-20).

Embodiments of the present invention as recited by the language of dependent claims of independent claim 21 contemplate the bus being characterized as a selected one of a serial

bus and a parallel bus (see pg. 2 line 25 to pg. 3 line 3). The first and second data can be characterized as being user data transferred between a host device and a storage medium (see pg. 11 lines 20-21). The user data can be transmitted via the bus between a read/write channel (such as 300, see pg. 8 lines 9-10) and a controller (such as 210, see pg. 8 lines 7-8). The first data can be transmitted at a first data rate and the second data transmitted at a second rate different than the first rate (such as block 35 between blocks 33 and 37 in FIG. 6, see pg. 9 lines 23-27).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-3, 5, 16, 18, 19, and 21-25 stand rejected under 35 U.S.C. §102 as allegedly being anticipated by U.S. 5,276,564 to Hessing ("Hessing '564").

Claims 16-20 stand rejected under 35 U.S.C. §101 as allegedly being directed to non-statutory subject matter.

VII. ARGUMENT

THE REJECTION OF INDEPENDENT CLAIMS 1, 16, AND 21 UNDER SECTION 102 AS ALLEGEDLY BEING ANTICIPATED BY HESSING '564 IS CLEAR ERROR BECAUSE THERE IS NO EVIDENCE IN THE RECORD THAT HESSING DISCLOSES TRANSFERRING DATA AND UPDATING A REGISTER OVER THE SAME BUS AS CLAIMED

Independent claims 1, 16, and 21 recite steps for performing different functions via a common bus. Particularly, these claims recite the following in pertinent part:

Claim 1, emphasis added

(a) retrieving a first portion of the recorded data via the bus;
(b) updating some of the registers via the bus; and
(c) retrieving a second portion of the recorded data via the bus.

Claim 16, emphasis added

(a) providing data via a bus;
(b) updating at least one register or parameter via the bus; and
(c) providing data via the bus responsive to the updating.

Claim 21, emphasis added

transmitting first data via a bus coupled to the processing device, updating at least one register or parameter via the bus, and transmitting second data via the bus in response to the updating step.

FIG.1 of Hessing '564 is helpful in understanding its disclosure.

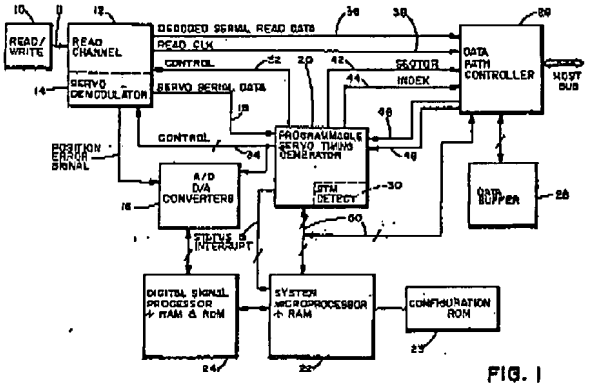


FIG. 1

Particularly, Hessing '564 discloses transferring data between the read channel 12 and the data path controller 26 via a decoded serial data stream 36 and associated synchronized clock signal 38. Hessing '564 further discloses passing data from ROM 23 to timing generator 20 to update registers 74, 76 via system data bus 50. Accordingly, Hessing '564 explicitly discloses transferring data and updating registers separately via the bus 50 and the serial data stream 36.[3]

During examination claims are given their "broadest reasonable interpretation consistent with the specification."[4] The "broadest reasonable interpretation" is the meaning that the skilled artisan would give to the claim term in view of the associated usage provided

[3] see Appellant's Pre-Brief Panel Request of 2/10/2007 ppg. 4-5; Appellant's Response of 12/11/2006, pg. 12; Appellant's Response of 7/24/2006, pg. 12

[4] *Phillips v. AWH Corp.*, 75 USPQ2d 1321 (Fed. Cir. 2005)(en Banc); MPEP 2111

in the specification.[5] A construction that is inconsistent with the written description would not be arrived at by the skilled artisan, and is therefore not a "reasonable interpretation."[6]

Appellant has argued that the term "bus" has plain meaning to the skilled artisan as that of a set of signal lines that interconnect components for communication among all or any subset of the components across the bus.[7] This meaning is consistent with the term's usage in the specification, where the bus 360 clearly interconnects the master IC 200 and slave IC 300 to the eblock 400.[8] Also, the extrinsic evidence introduced by the Examiner is consistent with this meaning:

> **bus** *n.* A set of hardware lines (conductors) used for data transfer among the components of a computer system. A buss is essentially a shared highway that connects different parts of the system – including the processor, disk-drive controller, memory, and input/output ports – and enables them to transfer information. The bus consists of specialized groups of lines that carry different types of information....[9]

However, the Examiner bases the rejection on a construction of the claim term *bus* to mean "all signal lines connecting items 12, 20, and 26." Appellant has pointed out in the record, without rebuttal by the Examiner, that there is no signal line in Hessing '564 that interconnects items 12, 20, and 26.[10] That is, with respect to the claimed data transfers and register updates over a common bus, the serial data stream 36 connects the read channel 12 and the controller 26, but is not connected to the timing generator 20; the system bus 50

---

[5] *In re American Academy of Science Technical Center*, 70 USPQ2d 1827 (Fed. Cir. 2004); *In re Cortright*, 49 USPQ2d 1463, 1468 (Fed. Cir. 1999); *In re Morris*, 44 USPQ2d 1023 (Fed. Cir. 1997)

[6] *Phillips, supra*; *In re Morris, supra*; *In re Zletz*, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989)

[7] see Appellant's Pre-Brief Panel Request of 2/10/2007, pg. 5; Appellant's Response of 12/11/2006, pg. 13

[8] see FIG. 3, pg. 8 lines 10-15

[9] Office Action of 10/11/2006, pg. 9 (emphasis added), citing *The Microsoft Computer Dictionary*

[10] see Appellant's Pre-Brief Panel Request of 2/10/2007 pg. 5; Appellant's Response of 12/11/2006, pg. 13; Appellant's Response of 7/24/2006, ppg. 13-14)

connects the controller 26 and the timing generator 20, but is not connected to the read channel 12.

Because there is no signal line interconnecting the read channel 12, timing generator 20, and controller 26, the Examiner's claim construction effectively is that the term "bus" means "any signal line connected to any one of the channel 12, timing generator 20, or controller 26."

Therefore, to affirm the Examiner's construction of the term "bus" as being reasonable, the Board must find that the skilled artisan would agree that the following seventeen signal lines in Hessing '564 would reasonably be viewed as a single bus:

line 11 between read/write apparatus and **channel 12**
serial data line 36 between **channel 12** and **controller 26**
clock signal 38 between **channel 12** and **controller 26**
control line 32 between **timing generator 20** and **channel 12**
control line 34 between **timing generator 20** and A/D and D/A converter 16 and between **timing generator 20** and **channel 12**
servo data line 18 between **channel 12** and **timing generator 20**
sector data line 42 between **timing generator 20** and **controller 26**
index data line 44 between **timing generator 20** and **controller 26**
read/write state line 46 between **controller 26** and **timing generator 20**
read/write state line 48 between **controller 26** and **timing generator 20**
system bus 50 between **controller 26** and **timing generator 20** and between **controller 26** and processor 22
line (not denoted) between **controller 26** data buffer 28
status and interrupt line between **timing generator 20** and processor 22
host bus connected to the **controller 26**
position error signal between the **channel 12** and the A/D and D/A converters

These seventeen signal lines are marked with an "X" inside a circle:

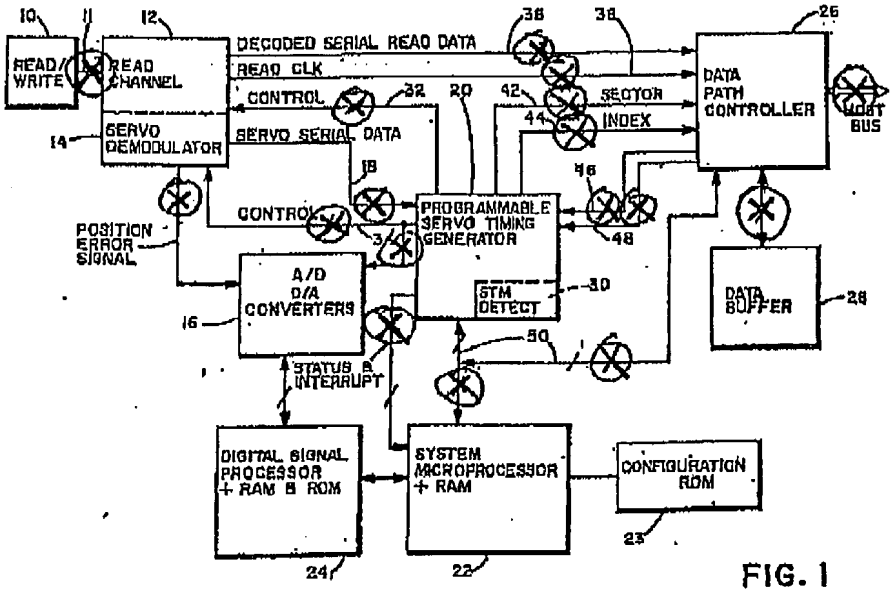


FIG. 1

Appellant respectfully believes the skilled artisan would think it absurd to say all these seventeen signal lines form a "bus" of any kind whatsoever. Furthermore, the Examiner's asserted meaning of "bus," that it means any signal line connected to any component, is not consistent with Hessing '564 or the specification. Hessing '564, for example, discloses separate signal lines 36, 38 instead of a bus for transferring the user data. Hessing '564 also explicitly discloses the system data bus 50, and does not even suggest that bus as including any of these other signal lines. The specification, for example, explicitly defines the bus 360 and does not even suggest that bus as including other signal lines such as line 350.

Rather, the plain meaning of "bus" in the context of the claim language and consistent with its usage in the specification would require a set of signal lines that interconnect the channel 12, timing generator 20, and controller 26 in Hessing '564 and capable of both transferring data and updating registers therebetween.

The Examiner's claim construction is clearly erroneous and reversible error for being unreasonably broad because it ignores the plain meaning of the term *bus* consistent with its usage in the specification, the knowledge of the skilled artisan, and the cited reference, thereby effectively ignoring explicitly recited claim terms.[11]

The Examiner's argument that his construction is reasonable "because the claims only require the components to be "operatively coupled" by the bus" is misplaced.[12] First, only claim 1 recites the term "operatively," claims 16 and 21 do not. Second, contrary to the Examiner's belief, Appellant's use of "operatively" does not relieve him of the obligation to construe the term "bus" no broader that the broadest reasonable construction. Rather, the term "operatively" is a descriptive term that is commonly used to reflect a functional relationship between claimed components. Absent any clear and unmistakable disavowal of claim scope, the term "operatively" in and of itself does nothing to take away from the full breath of the claim term's ordinary meaning.[13] Thus, the fact that the bus is "operatively coupled" to the controller chip and the channel chip in claim 1 means that they must be coupled in a manner capable of performing the function of both retrieving data and updating a register.

To find anticipation there must be evidence of a single prior art reference that identically discloses all the recited claim elements, and the elements must be arranged as required by the claim.[14] Here, the Examiner has offered no evidence whatsoever that substantiates a reasonable basis for his construction that Hessing '564 both transfers data and updates registers over a common "bus" as is generally claimed by independent claims 1, 16,

---

[11] *in Re Morris, supra*

[12] Advisory Action of 1/9/2007, pg. 2

[13] *Innova/Pure Water Inc. v. Safari Water Filtration Sys. Inc.*, 72 USPQ2d 1001, 1008 (Fed. Cir. 2004)

[14] *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990)

and 21. Therefore, the Section 102 rejection is reversible error for being unsubstantiated because there is no evidence in the record that Hessing '564 discloses all the features of independent claims 1, 16, and 21. Appellant respectfully requests that the final rejection of claims 1, 16, and 21 and the claims depending therefrom be reversed.

THE REJECTION OF INDEPENDENT CLAIM 16 UNDER SECTION 101 FOR ALLEGEDLY RECITING NON-STATUTORY LANGUAGE IS CLEAR ERROR BECAUSE THERE IS NO EVIDENCE IN THE RECORD SUBSTANTIATING THE REJECTION

By reviewing the protracted prosecution history of this case the Board will see that Appellant has been forced to draft this Brief without the benefit of a substantiated basis for the Section 101 rejection of claim 16. Particularly, for the first 22 months of prosecution the Examiner deemed its language to pass statutory muster because the rejections were all under Sections 102 and 103, not Section 101.[15] Appellant successfully obviated all those rejections.[16]

If this case actually were in condition for appeal, then the circumstances of this case could simply be attributed to an implicit admission by the Examiner that the first four examinations of claim 16 were incomplete, because a complete examination goes to the merits of the claims both with respect to statutory compliance and patentability.[17] However, unfortunately the Board will find that like the first four Section 102 rejections, the three Section 101 rejections were likewise wholly unsubstantiated.

The Examiner's first basis for the Section 101 rejection was that claim 16 lies within a judicial exception to the statutory categories because "it can be easily construed as an

[15] First rejection was a Section 103 rejection over Bowes and Cloke (see Office Action of 3/16/2004, pg. 9). Second rejection was a Section 102 rejection over Cloke (see Office Action of 11/5/2004, ppg. 3-4). Third and fourth rejections were a Section 102 rejection over Liu (see Office Actions of 5/12/2005 and 10/25/2005).
[16] See Appellant's Responses of 6/16/2004, 3/4/2005, and 12/27/2005.
[17] 37 C.F.R. 1.104(a)

abstract idea...."[18] The Examiner's second basis for the Section 101 rejection was that claim 16 lies within a judicial exception to the statutory categories because it "lacks practical application because the claims have no concrete or useful application/result."[19] Appellant successfully obviated both of those bases.[20]

The Examiner's third basis for the Section 101 rejection was that it is "an attempt to claim every practical application of updating a register over a bus, and is therefore preempting that abstract idea and non-statutory."[21] Appellant traversed that basis by pointing out that MPEP 2106 clearly requires that "If USPTO personnel determine that the claimed invention preempts a 35 U.S.C. 101 judicial exception, they must identify the abstraction, law of nature, or natural phenomenon and explain why the claim covers every substantial practical application thereof.[22] The Examiner's third stated basis fails to substantiate any evidence meeting this requisite burden for establishing non-patentable subject matter.

Neither the Examiner nor the Pre-Brief Panel rebutted Appellant's traversal of the third basis for the Section 101 rejection. As a result, Appellant is placed in the untenable position of drafting this Brief without knowing a bona fide basis for the Section 101 rejection. Appellant can only hope that the Examiner will either reopen the merits or finally substantiate the Section 101 rejection in his Answer.

Appellant believes that the Board can only reasonably conclude that the Examiner has failed to substantiate evidence in the record that it is more likely than not that the claimed invention as a whole either falls outside of one of the enumerated statutory classes or within one of the exceptions to statutory subject matter. Accordingly, the Board should

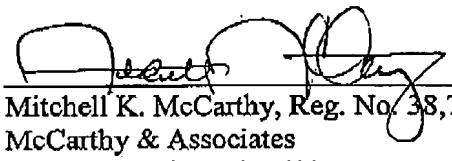
[18] Office Action of 1/24/2006 pg. 2
[19] Office Action of 10/11/2006 pg. 2
[20] see Appellant's Response of 7/24/2006, pg. 11; Appellant's Response of 7/24/2006, pg. 11
[21] Advisory Action of 1/9/2007, pg. 2
[22] MPEP 2106(IV)(C)(3), see Appellant's Pre-Brief Panel Request of 2/10/2007 ppg. 3-4

treat the rejection of claim 16 as reversible error, and as such reverse the rejection of claim 16 and the claims depending therefrom.

Conclusion

In conclusion, Appellant respectfully requests that the rejection of all pending claims be reversed.

Respectfully submitted,

By: 

Mitchell K. McCarthy, Reg. No. 38,794
McCarthy & Associates
500 West Main, Suite 609
Oklahoma City, Oklahoma 73102
Telephone: (405) 601-2798
Facsimile: (405) 601-2853

VIII. CLAIMS APPENDIX

1. (Previously presented) In an apparatus having a bus operatively coupled to a first controller chip and a first channel chip, the channel chip having several registers, the apparatus also having a storage medium operatively coupled to the bus through a storage medium interface, a method for retrieving data recorded on the storage medium comprising steps of:

(a) retrieving a first portion of the recorded data via the bus;

(b) updating some of the registers via the bus; and

(c) retrieving a second portion of the recorded data via the bus.

2. (Original) The method of claim 1 in which the interface includes a read head, further comprising a step (d) of repositioning the storage medium interface with respect to the storage medium, between retrieving steps (a) and (c).

3. (Original) The method of claim 2 in which the interface has a plurality of operating parameters that are modified in updating step (b).

4. (Previously presented) The method of claim 1 in which the registers contain at least one read channel parameter value selected from the group consisting of: a precompensation value, a filter coefficient value, and a phase offset value.

5. (Previously presented) The method of claim 1 in which the registers contain at least one mode-indicative value.

6. (Original) In a storage system having a disc with at least two zones having zone identifiers Z_A and Z_B, an interface configured to read data in zone Z_A, a target segment in zone Z_B, a value table indexed by zone identifiers, a direct memory access (DMA) controller, a microprocessor coupled to the DMA controller, and several read channel registers each containing a value, a method comprising steps of:

(a) retrieving via the DMA controller several values indexed by zone identifier Z_B;

(b) updating at least some of the read channel register values from the retrieved values;

(c) reconfiguring the interface to read data in zone Z_B; and

(d) reading the target segment.

7. (Original) The method of claim 6 in which the target segment has a predetermined starting track number, further comprising a step of deriving zone identifier Z_B from the predetermined starting track number before retrieving step (a).

8. (Original) The method of claim 6 in which the interface includes at least one head, in which positioning step (c) includes a step of (c1) moving the at least one head radially across the disc, the moving step (c1) beginning before retrieving step (a) is complete.

9. (Original) The method of claim 8 in which moving step (c1) begins before retrieving step (a) begins.

10. (Original) The method of claim 6 in which zone Z_B has a corresponding data rate R_B that is not in common with zone Z_A, in which positioning step (c) includes a step of (c2) sampling a signal from the interface at an initial frequency that is an integer multiple of data rate R_B.

11. (Original) The method of claim 6 further comprising prior steps of:

(e) configuring the interface to read data in zone Z_B;

(f) receiving a signal from the interface;

(g) deriving several values indicative of the interface's performance in zone Z_B from the received signal; and

(h) storing some of the derived values in the value table each at a position associated with zone Z_B.

12. (Original) The method of claim 6 in which the storage system includes an integrated circuit comprising the microprocessor, and in which the retrieving step (a) comprises issuing at least one but fewer than 10 commands from the microprocessor to the DMA controller.

13. (Original) The method of claim 12 further comprising steps of:

(j) sensing position data from a servo sector via the interface; and

(k) deriving a servo control signal from the sensed position data with the microprocessor during step (b).

14. (Original) The storage system of claim 6 configured to perform the method of claim 6 further comprising a printed circuit board assembly including a memory containing the value table, the storage system comprising:

a master integrated circuit (IC) containing the microprocessor and the direct memory access (DMA) controller, the DMA controller being operatively coupled to the memory;

a slave IC containing the several read channel registers; and

a bus coupled between the master IC and the slave IC, the bus controllable by the DMA controller to perform updating step (b).

15. (Previously presented) An apparatus comprising:

an interface configured to read data from a storage medium;

a memory containing several values indexed by zone identifiers;

a first controller chip containing a microprocessor and a direct memory access (DMA) controller, the DMA controller operatively coupled to the memory;

a first channel chip having several registers; and

a bus operatively coupled between the interface and the chips, the bus controllable by the DMA controller to read from the memory and to update several of the registers in response to a zone transition event.

16. (Previously presented) A method comprising steps of:

(a) providing data via a bus;

(b) updating at least one register or parameter via the bus; and

(c) providing data via the bus responsive to the updating.

17. (Previously presented) The method of claim 16 wherein the bus is serial.

18. (Previously presented) The method of claim 16 wherein the bus is parallel.

19. (Previously presented) The method of claim 16 wherein the steps are controlled by a processor.

20. (Previously presented) The method of claim 16 wherein the steps are controlled by a direct memory access apparatus.

21. (Previously presented) A method for reducing processing burden on a processing device, comprising steps of transmitting first data via a bus coupled to the processing device, updating at least one register or parameter via the bus, and transmitting second data via the bus in response to the updating step.

22. (Previously presented) The method of claim 21 wherein the bus is characterized as a selected one of a serial bus or a parallel bus.

23. (Previously presented) The method of claim 21 wherein the first and second data are respectively characterized as user data transferred between a host device and a storage medium.

24. (Previously presented) The method of claim 23, wherein the user data are transmitted via the bus between a read/write channel and a controller.

25. (Previously presented) The method of claim 21, wherein the first data are transmitted at a first data rate and the second data are transmitted at a second rate different than the first rate.

IX. EVIDENCE APPENDIX

No additional evidence is included.

X. RELATED PROCEEDINGS APPENDIX

There exist no relevant related proceedings concerning this Appeal before the Board.